

Notice of References Cited	Application/Control No. 10/731,000		Applicant(s)/Patent Under Reexamination MONOE ET AL.	
	Examiner Evan Pert		Art Unit 2826	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,933,184 B2	08-2005	Arao et al.	438/163
	B	US-6,872,604 B2	03-2005	Yamazaki et al.	438/151
	C	US-6,706,544 B2	03-2004	Yamazaki et al.	438/30
	D	US-6,596,571 B2	07-2003	Arao et al.	438/163
	E	US-2004/0140472 A1	07-2004	Fujimoto et al.	257/072
	F	US-2003/0100151 A1	05-2003	Okamoto, Satoru	438/163
	G	US-2003/0062524 A1	04-2003	Kimura, Hajime	257/72
	H	US-2003/0020118 A1	01-2003	Kajiwara et al.	257/347
	I	US-2002/0163049 A1	11-2002	Yamazaki et al.	257/408
	J	US-2001/0048408 A1	12-2001	Koyama et al.	345/76
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)			
	U	Mishima et al., "Improved Lifetime of Poly-Si TFTs with a Self-aligned Gate-overlapped LDD Structure", June 2002, IEEE Transactions on Electron Devices, Vol. 49, No. 6, pages 981-985.			
	V	Ohgata et al., "A new dopant activation technique for poly-Si TFTs with a self-aligned gate-overlapped LDD structure", December 2000, IEDM Technical Digest, pages 205-208.			
	W				
	X				

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.